具有 ±250mV 输入电压、3μs 延迟的增强隔离式 AMC1301 精密放大器

1 特性

- 针对使用分流电阻的电流测量优化了 ±250mV 输入电压范围
- 低偏移误差和漂移：
  25°C 时为 ±200μV，±3 μV/°C
- 固定增益 = 8.2
- 超低增益误差和漂移：
  25°C 时为 ±0.3%，±50ppm/°C
- 超低非线性度和漂移：
  0.03%，1ppm/°C
- 高侧和低侧以 3.3V 电压运行
- 系统级诊断 特性
- 安全相关认证：
  - 7000 V_{PK} 增强型隔离，符合 DIN V VDE-V 0884-10 (VDE-V 0884-10): 2006-12 标准
  - 符合 UL 1577 标准且长达 1 分钟的 5000 V_{RMS} 隔离
  - CAN/CSA No. 5A 组件接受服务通知、IEC 60950-1 和 IEC 60065 终端设备标准
- 可在扩展工业温度范围内运行

2 应用

- 基于分流电阻的电流感测用于下列应用：
  - 电机驱动器
  - 变频器
  - 不间断电源
- 隔离电压感测

3 说明

AMC1301 器件是一款隔离式精密放大器，此放大器的输出与输入电路由抗电磁干扰性能极强的隔离层隔开。根据 VDE V 0884-10 和 UL1577 标准，该隔离栅经认证可提供高达 7 kV_{PEAK} 的增强型电流隔离。当与隔离电源配合使用时，该器件可防止共模高电压线路上的噪声电流流入本地接地并干扰或损害敏感电路。

AMC1301 器件的输入针对直接连接分流电阻器或其他低电压等级信号源的情况进行了优化。该器件性能优异，支持精确电流控制，从而降低系统级功耗（尤其在电机控制应用中）并减少扭矩纹波。该 器 件 (AMC1301) 的集成共模过压和高侧电源电压缺失检测特性可简化系统级设计和诊断。

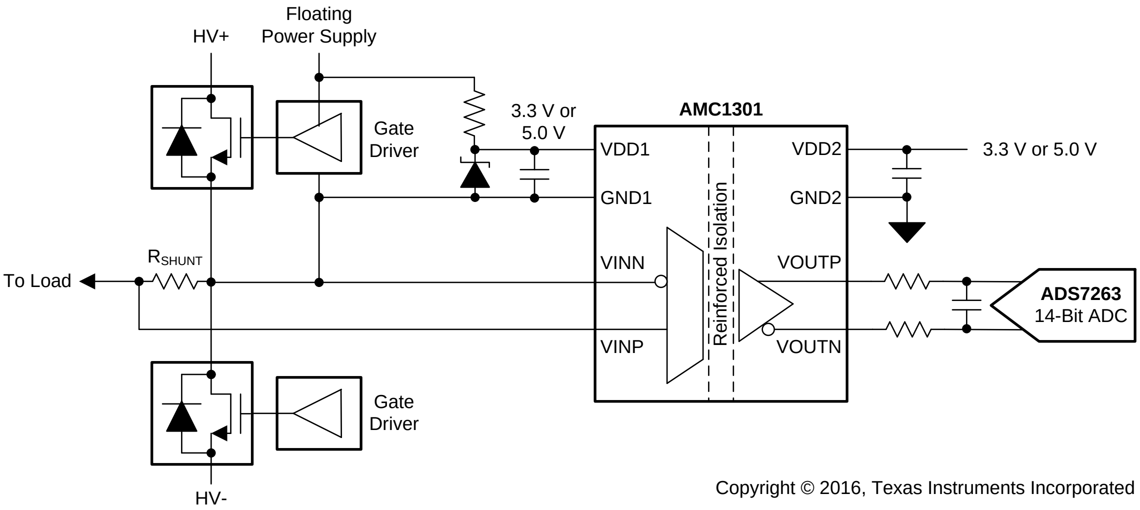
AMC1301 器件在扩展工业温度范围内（–40°C 到 +125°C）完全额定运行，并采用宽体 8 引脚 SOIC (DWV) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
AMC1301	SOIC (8)	5.85mm × 7.50mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化电路原理图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (September 2016) to Revision D

Page

- Changed *VDD1* to *VDD2* in test conditions of I_{DD2} and P_{DD2} parameters of *Electrical Characteristics* table 8
- 已更改 *VDD2* to *VDD1* in conditions of *Gain Error Histogram* figures 12

Changes from Revision B (June 2016) to Revision C

Page

- 将*简化原理图* 中的 *12 位 ADC* 更改为 *14 位 ADC* 1
- Changed maximum specification of *Supply voltage* row in *Absolute Maximum Ratings* table 5
- Changed *12-Bit ADC* to *14-Bit ADC* in *Zener-Diode Based, High Side Power Supply* figure in *Power Supply Recommendations* section 25

Changes from Revision A (April 2016) to Revision B

Page

- 已更改 特性 要点“安全及管理批准”至“安全相关认证” 1
- 更改了*器件信息* 表中的*简化原理图* 1
- Changed section title from "Regulatory Information" to "Safety-Related Certifications" 7
- Changed V_{CM} test conditions in *Electrical Characteristics* table 7
- Added V_{IN} footnote to *Electrical Characteristics* table 7
- Changed V_{IN} test conditions in *Electrical Characteristics* table 7
- Changed V_{IN} units in *Electrical Characteristics* table 7
- Changed common-mode rejection ratio test condition in *Electrical Characteristics* table 7
- Changed R_{IN} parameter information in *Electrical Characteristics* table 7
- Changed output noise equation in *Electrical Characteristics* table 8
- 已删除 "Safety and" from *Insulation Characteristics Curves* section title 9
- 已更改 *Using the AMC1301 Device for Current Sensing in Frequency Inverters* figure in *Application Information* 20

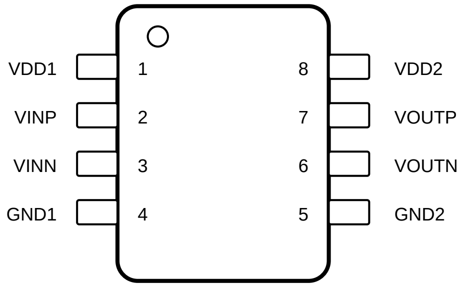
- 已更改 *Zener-Diode Based, High Side Power Supply* figure in *Power Supply Recommendations* 25
- 已添加 一段内容并更改了*相关文档*部分的格式.. 27

Changes from Original (April 2016) to Revision A — Page

- 已发布为量产数据 1

5 Pin Configuration and Functions

DWV Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	4	—	High-side analog ground
GND2	5	—	Low-side analog ground
VDD1	1	—	High-side power supply, 3.0 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.
VDD2	8	—	Low-side power supply, 3.0 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.
VINN	3	I	Inverting analog input
VINP	2	I	Noninverting analog input
VOUTN	6	O	Inverting analog output
VOUTP	7	O	Noninverting analog output

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Supply voltage, VDD1 to GND1 or VDD2 to GND2	–0.3	7	V
Analog input voltage at VINP, VINN	GND1 – 6	VDD1 + 0.5	V
Input current to any pin except supply pins	–10	10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD1	High-side supply voltage (VDD1 to GND1)	3.0	5.0	5.5	V
VDD2	Low-side supply voltage (VDD2 to GND2)	3.0	3.3	5.5	V
T_A	Operating ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		AMC1301	UNIT
		DWV (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*, SPRA953.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	81.4	mW
P_{D1}	Maximum power dissipation (high-side supply)		45.65	mW
P_{D2}	Maximum power dissipation (low-side supply)		35.75	mW

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 9	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 9	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2 × 0.0135 mm)	≥ 0.027	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	
DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At ac voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At ac voltage (sine wave)	1000	V_{RMS}
		At dc voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7000	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8400	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 10000\ V_{PK}$ (qualification)	6250	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM} = 1800\ V_{PK}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM} = 2400\ V_{PK}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM} = 2812.5\ V_{PK}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	$V_{IO} = 0.5\ V_{PP}$ at 1 MHz	1.2	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_S = 150°C	$> 10^9$	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$ or 7000 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.

(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

6.8 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O may allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 110.1°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			206	mA
		θ_{JA} = 110.1°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			315	
P_S	Safety input, output, or total power	θ_{JA} = 110.1°C/W, T_J = 150°C, T_A = 25°C			1135(1)	mW
T_S	Maximum safety temperature				150	°C

(1) Input, output, or the sum of input and output power must not exceed this value.

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics

Minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, VINP = –250 mV to +250 mV, and VINN = 0 V. Typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	VINP – VINN		±302.7		mV
V_{FSR}	Specified linear differential full-scale	VINP – VINN	–250		250	mV
V_{CM}	Specified common-mode input voltage	(VINP + VINN) / 2 to GND1	–0.16		VDD1 – 2.1	V
	Absolute common-mode input voltage(1)	(VINN + VINP) / 2 to GND1	–2		VDD1	V
V_{CMov}	Common-mode overvoltage detection level		VDD1 – 2			V
V_{OS}	Input offset voltage	Initial, at T_A = 25°C, VINP = VINN = GND1	–200	±50	200	µV
TCV_{OS}	Input offset drift		–3	±1	3	µV/°C
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–93		dB
		f_{IN} = 10 kHz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–93		
C_{IND}	Differential input capacitance			1		pF
R_{IN}	Single-ended input resistance	VINN = GND1		18		kΩ
R_{IND}	Differential input resistance			22		kΩ
I_{IB}	Input bias current	VINP = VINN = GND1	–82	–60	–48	µA
TCI_{IB}	Input bias current drift			1		nA/°C
BW_{IN}	Input bandwidth			1000		kHz

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in *Absolute Maximum Ratings*.

Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, VINP = –250 mV to +250 mV, and VINN = 0 V. Typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
	Nominal gain			8.2		
E_G	Gain error	Initial, at T_A = 25°C	–0.3%	±0.05%	0.3%	
TCE_G	Gain error drift		–50	±15	50	ppm/°C
	Nonlinearity		–0.03%	±0.01%	0.03%	
	Nonlinearity drift			1		ppm/°C
THD	Total harmonic distortion	f_{IN} = 10 kHz		–87		dB
	Output noise	VINP = VINN = GND1, f_{IN} = 0 Hz, BW = 100 kHz		220		μV_{RMS}
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, BW = 10 kHz	80	84		dB
		f_{IN} = 10 kHz, BW = 100 kHz		71		
PSRR	Power-supply rejection ratio	vs VDD1, at dc		–94		dB
		vs VDD1, 100-mV and 10-kHz ripple		–90		
		vs VDD2, at dc		–100		
		vs VDD2, 100-mV and 10-kHz ripple		–94		
t_r	Rise time	See 图 45		2.0		µs
t_f	Fall time	See 图 45		2.0		µs
	V_{IN} to V_{OUT} signal delay (50% – 10%)	See 图 46, unfiltered output		0.7	2.0	µs
	V_{IN} to V_{OUT} signal delay (50% – 50%)	See 图 46, unfiltered output		1.6	2.6	µs
	V_{IN} to V_{OUT} signal delay (50% – 90%)	See 图 46, unfiltered output		2.5	3.0	µs
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1 kV	15			kV/µs
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
	Output short-circuit current			±13		mA
R_{OUT}	Output resistance	on VOUTP or VOUTN		< 0.2		Ω
BW	Output bandwidth		190	210		kHz
$V_{FAILSAFE}$	Failsafe differential output voltage	$V_{CM} \geq V_{CMov}$, or VDD1 missing		–2.563	–2.545	V
POWER SUPPLY						
I_{DD1}	High-side supply current	3.0 V ≤ VDD1 ≤ 3.6 V		5.0	6.9	mA
		4.5 V ≤ VDD1 ≤ 5.5 V		5.9	8.3	
I_{DD2}	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V		4.4	5.6	mA
		4.5 V ≤ VDD2 ≤ 5.5 V		4.8	6.5	
P_{DD1}	High-side power dissipation	3.0 V ≤ VDD1 ≤ 3.6 V		16.5	24.84	mW
		4.5 V ≤ VDD1 ≤ 5.5 V		29.5	45.65	
P_{DD2}	Low-side power dissipation	3.0 V ≤ VDD2 ≤ 3.6 V		14.52	20.16	mW
		4.5 V ≤ VDD2 ≤ 5.5 V		24	35.75	

6.10 Insulation Characteristics Curves

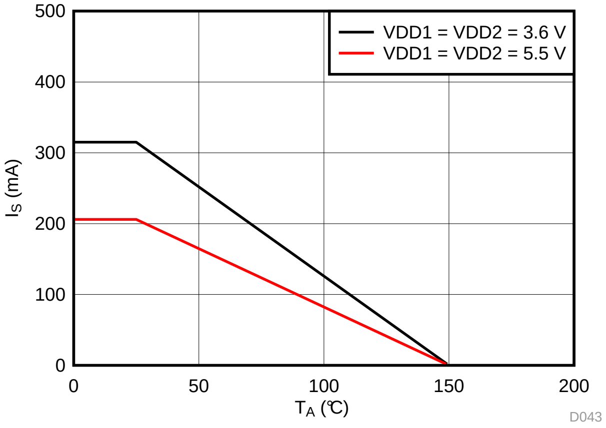


图 1. Thermal Derating Curve for Safety-Limiting Current per VDE

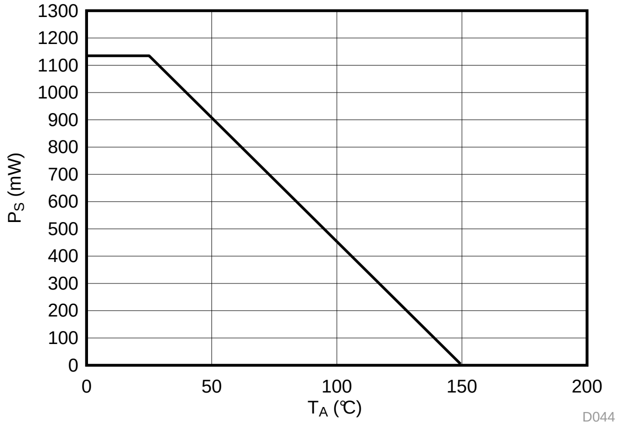
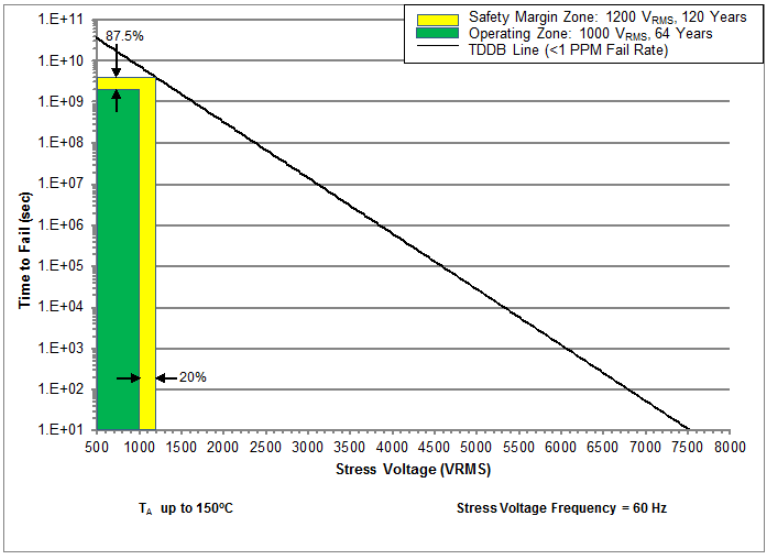


图 2. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress voltage frequency = 60 Hz

图 3. Reinforced Isolation Capacitor Lifetime Projection

6.11 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

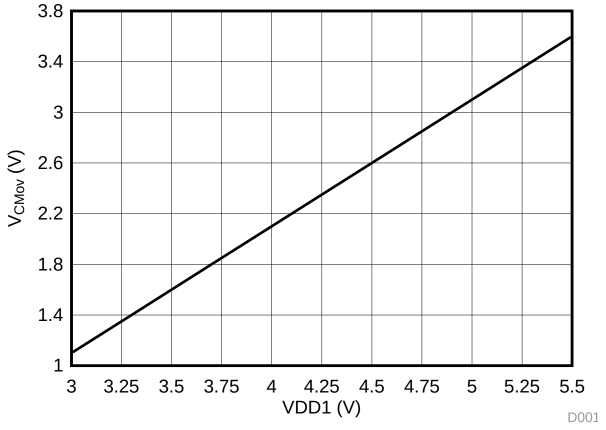


图 4. Common-Mode Overvoltage Detection Level vs High-Side Supply Voltage

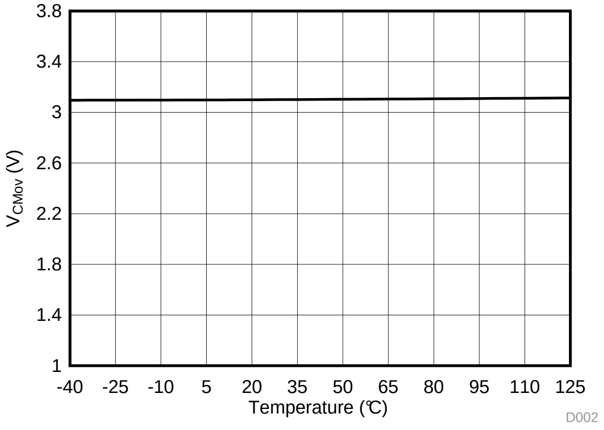
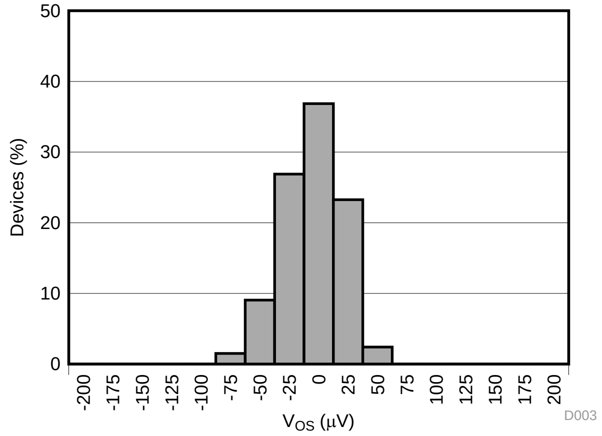
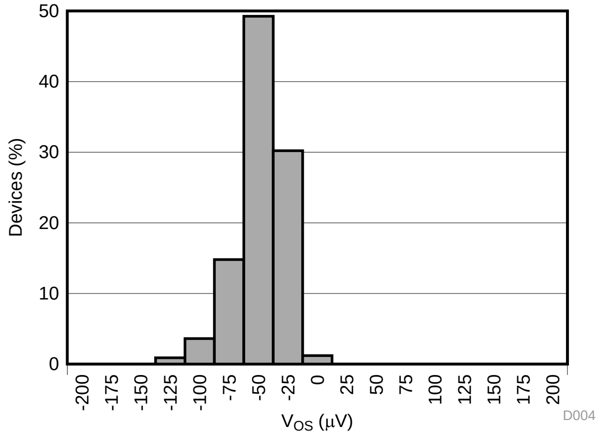


图 5. Common-Mode Overvoltage Detection Level vs Temperature



VDD1 = 3.3 V

图 6. Input Offset Voltage Histogram



VDD1 = 5 V

图 7. Input Offset Voltage Histogram

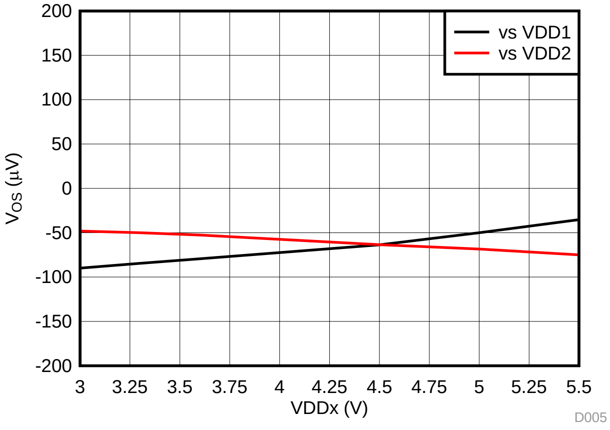


图 8. Input Offset Voltage vs Supply Voltage

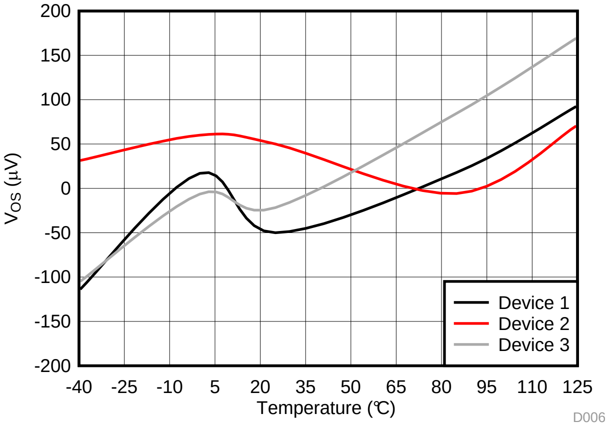


图 9. Input Offset Voltage vs Temperature

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

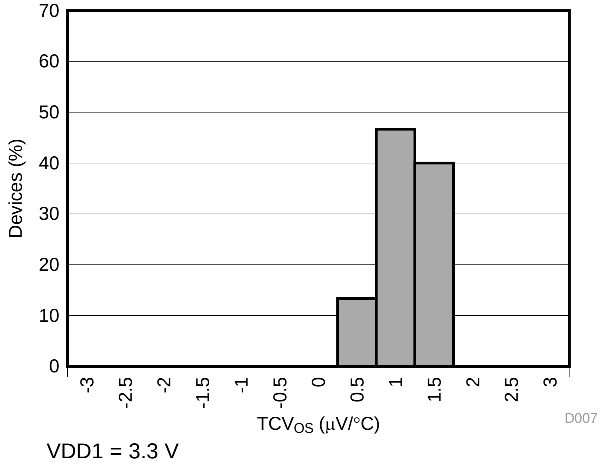


图 10. Input Offset Drift Histogram

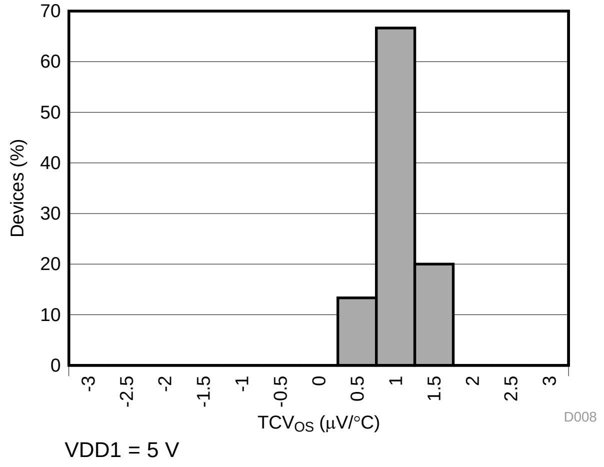


图 11. Input Offset Drift Histogram

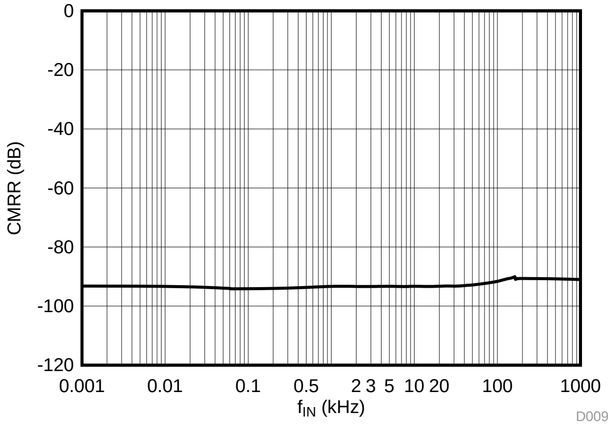


图 12. Common-Mode Rejection Ratio vs Input Frequency

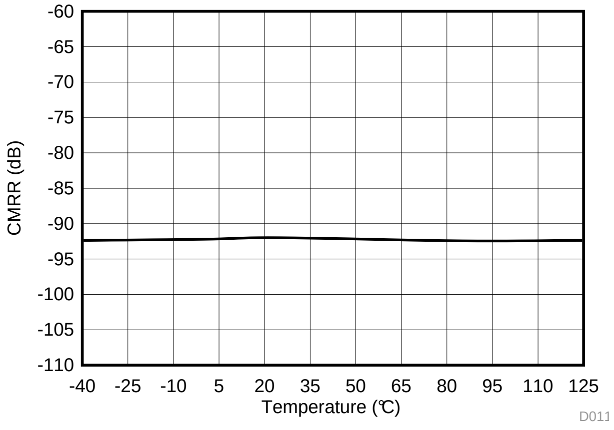


图 13. Common-Mode Rejection Ratio vs Temperature

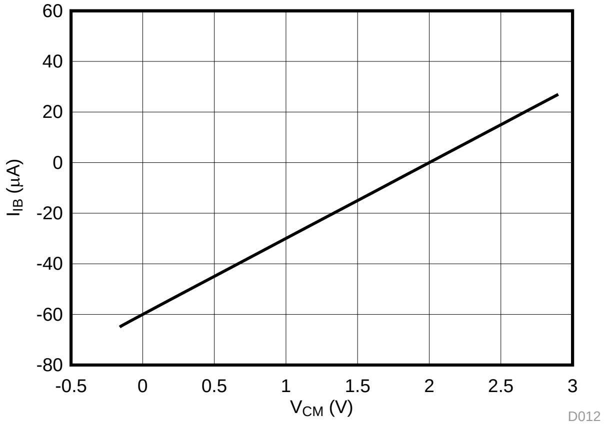


图 14. Input Bias Current vs Common-Mode Input Voltage

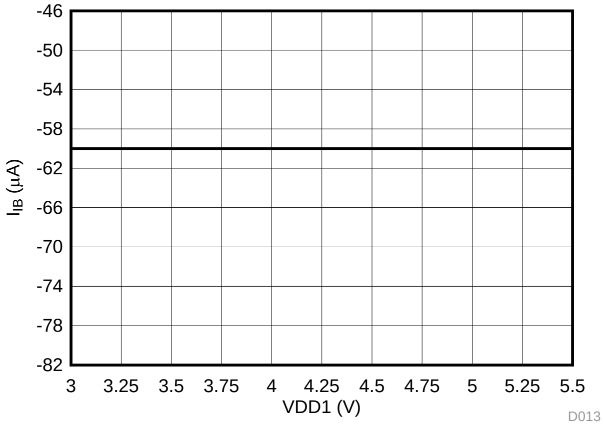


图 15. Input Bias Current vs High-Side Supply Voltage

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

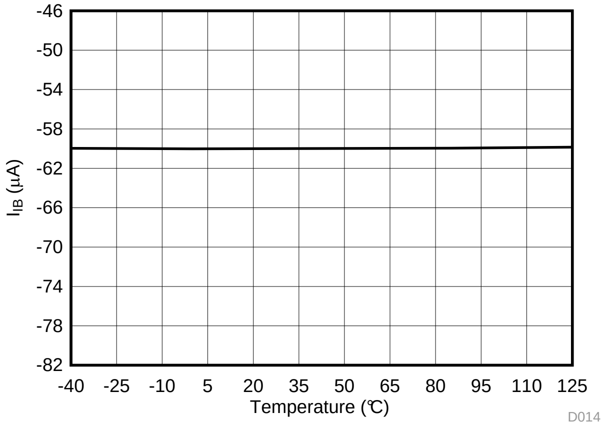


图 16. Input Bias Current vs Temperature

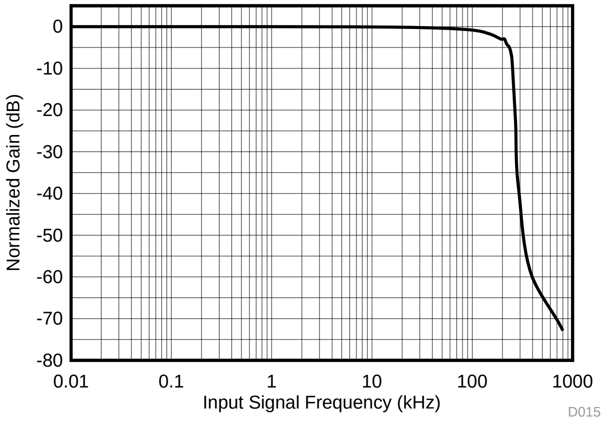
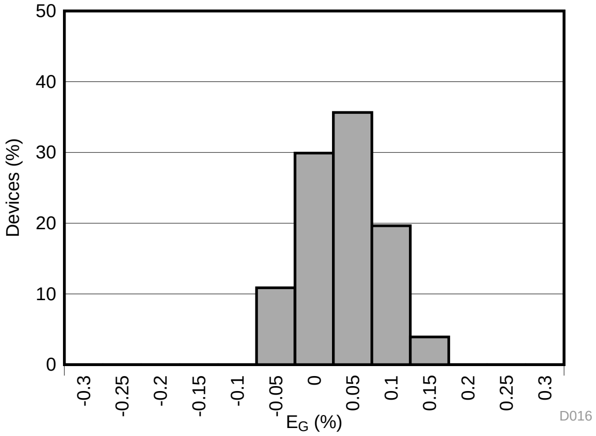
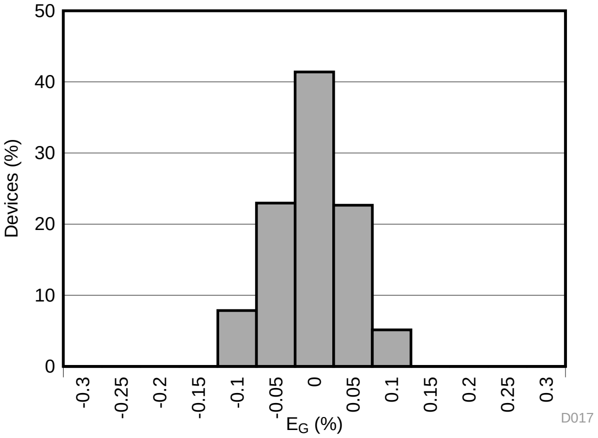


图 17. Normalized Gain vs Input Frequency



VDD1 = 3.3 V

图 18. Gain Error Histogram



VDD1 = 5 V

图 19. Gain Error Histogram

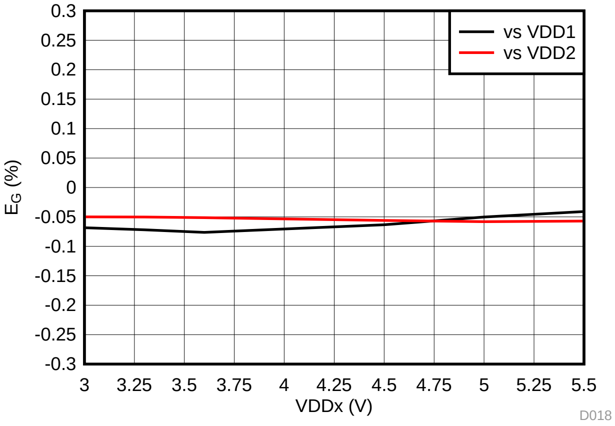


图 20. Gain Error vs Supply Voltage

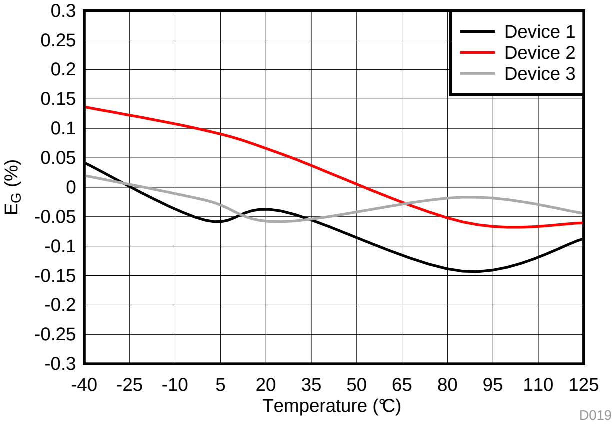
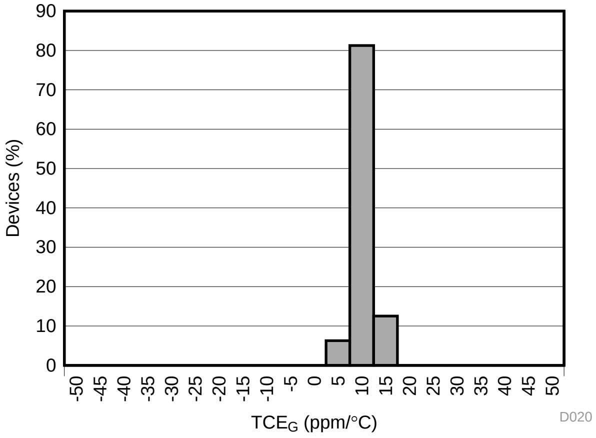


图 21. Gain Error vs Temperature

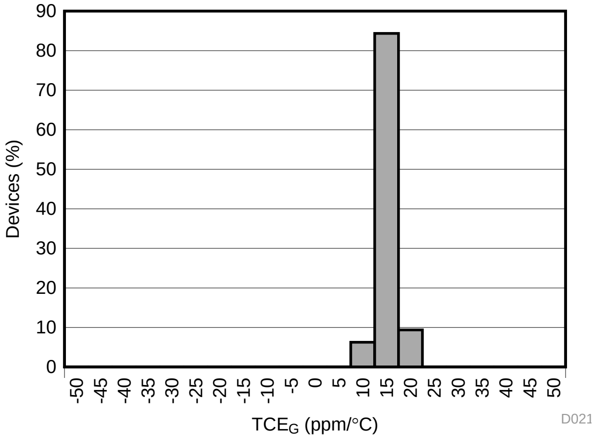
Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



VDD1 = 3.3 V

图 22. Gain Error Drift Histogram



VDD1 = 5 V

图 23. Gain Error Drift Histogram

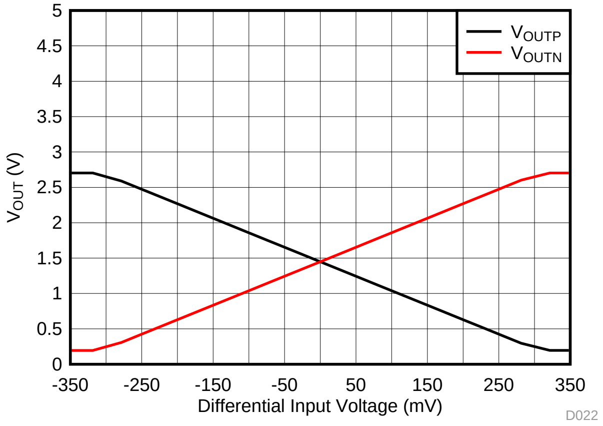


图 24. Output Voltage vs Input Voltage

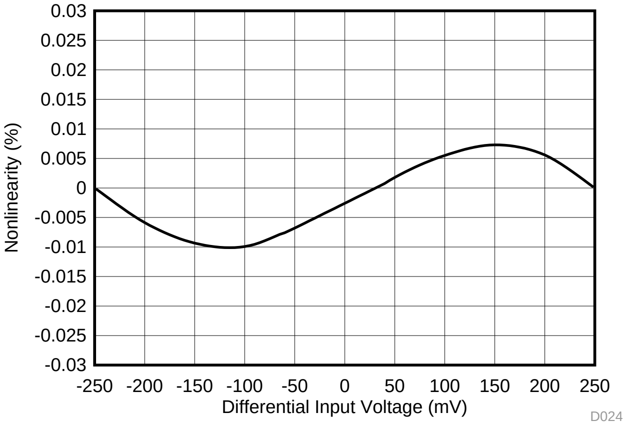


图 25. Nonlinearity vs Input Voltage

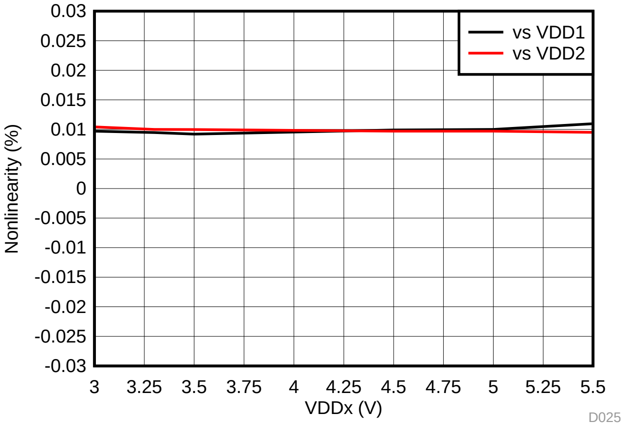


图 26. Nonlinearity vs Supply Voltage

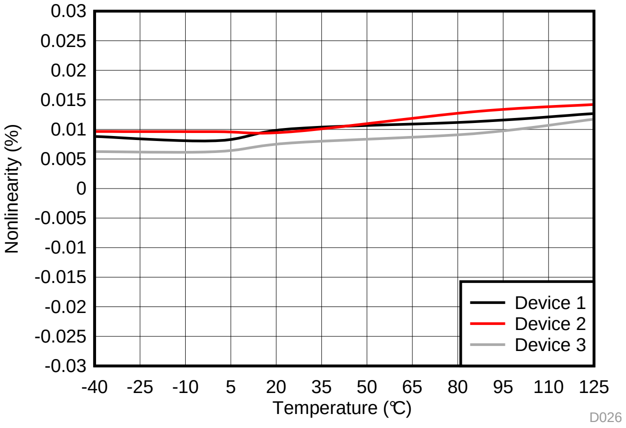


图 27. Nonlinearity vs Temperature

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

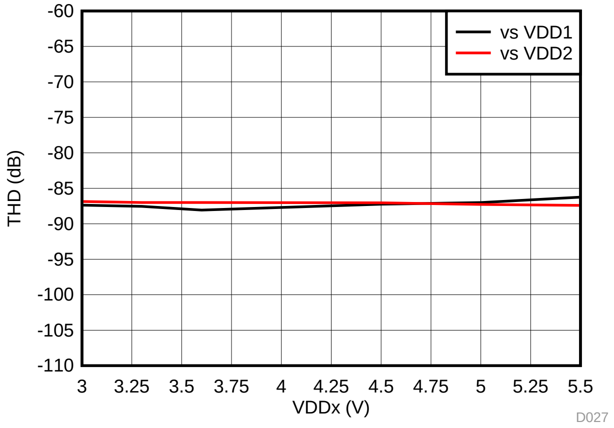


图 28. Total Harmonic Distortion vs Supply Voltage

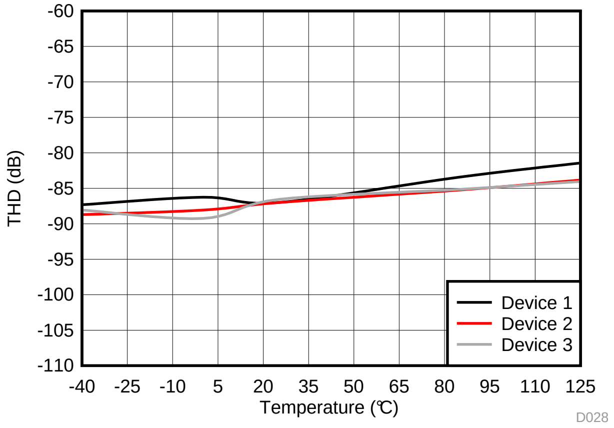


图 29. Total Harmonic Distortion vs Temperature

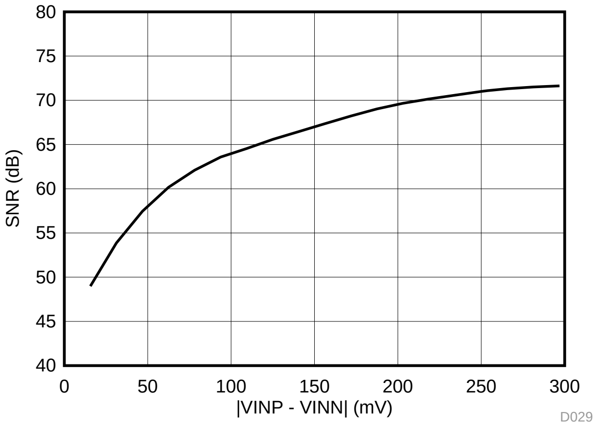


图 30. Signal-to-Noise Ratio vs Input Voltage

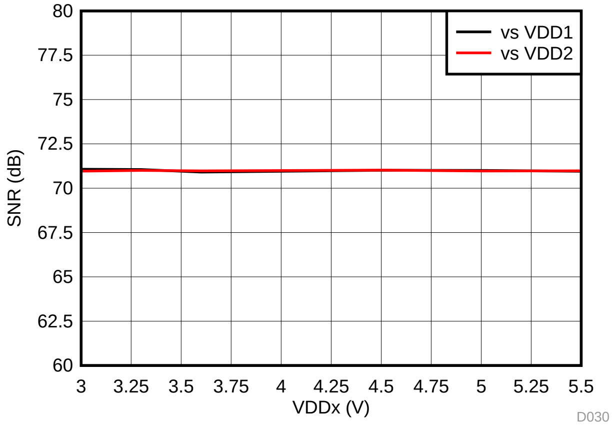


图 31. Signal-to-Noise Ratio vs Supply Voltage

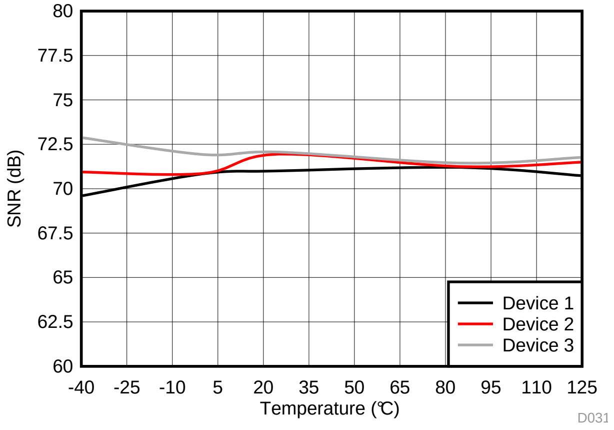


图 32. Signal-to-Noise Ratio vs Temperature

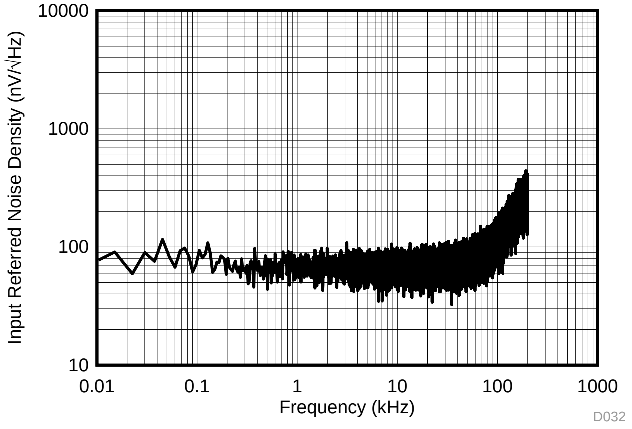
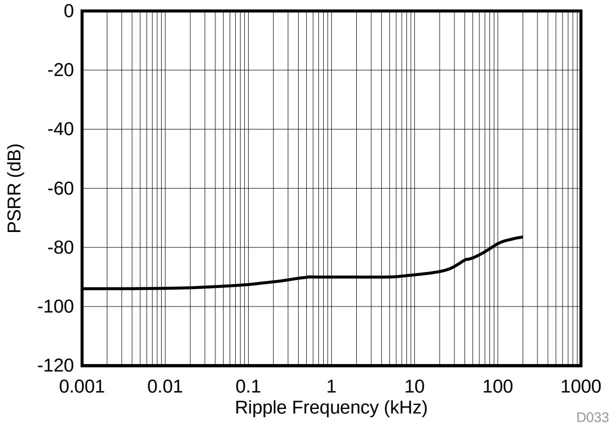


图 33. Input-Referred Noise Density vs Frequency

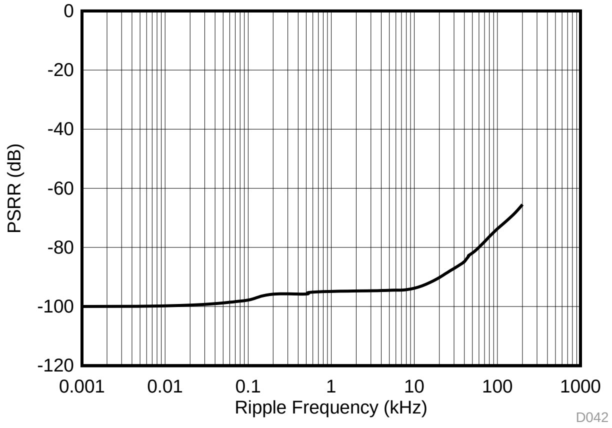
Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



vs VDD1

图 34. Power-Supply Rejection Ratio vs Ripple Frequency



vs VDD2

图 35. Power-Supply Rejection Ratio vs Ripple Frequency

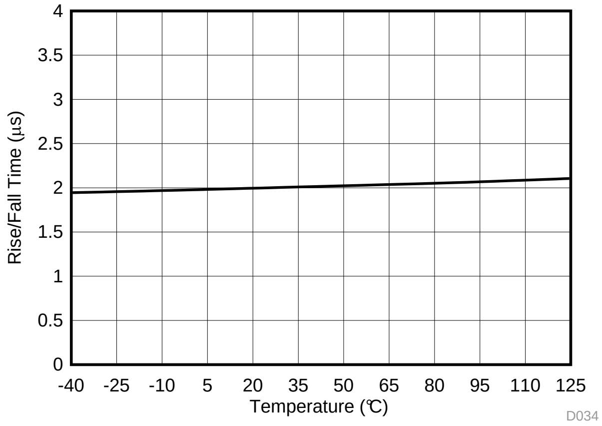


图 36. Output Rise and Fall Time vs Temperature

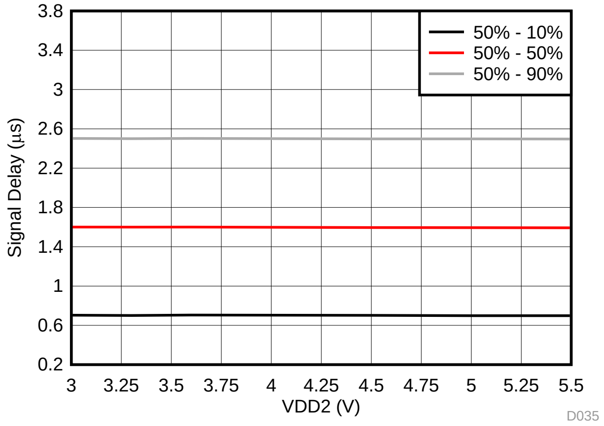


图 37. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

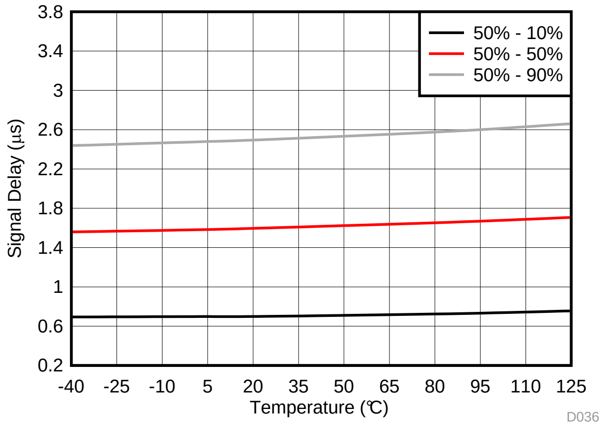


图 38. V_{IN} to V_{OUT} Signal Delay vs Temperature

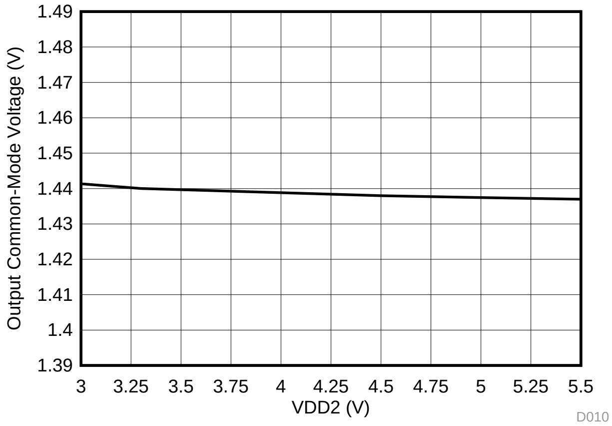


图 39. Output Common-Mode Voltage vs Low-Side Supply Voltage

Typical Characteristics (接下页)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

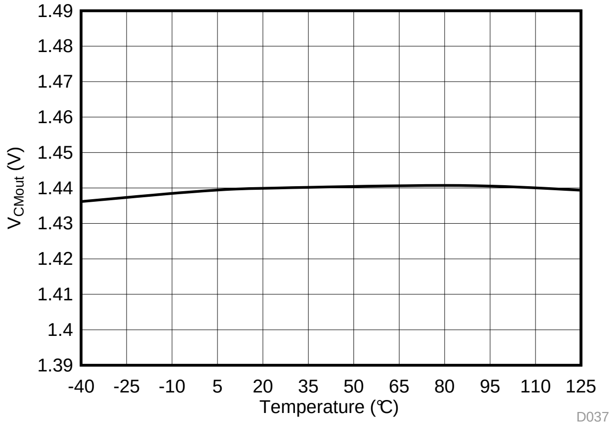


图 40. Output Common-Mode Voltage vs Temperature

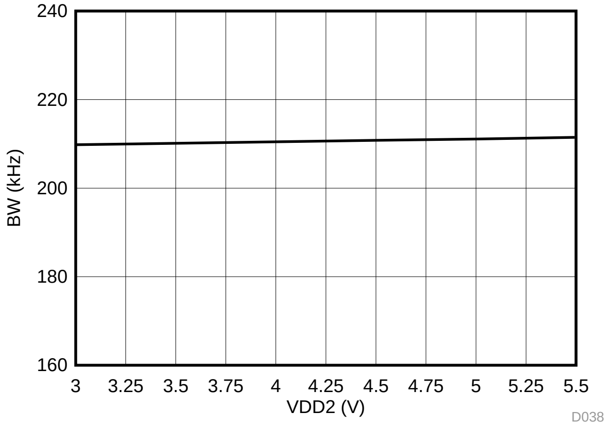


图 41. Output Bandwidth vs Low-Side Supply Voltage

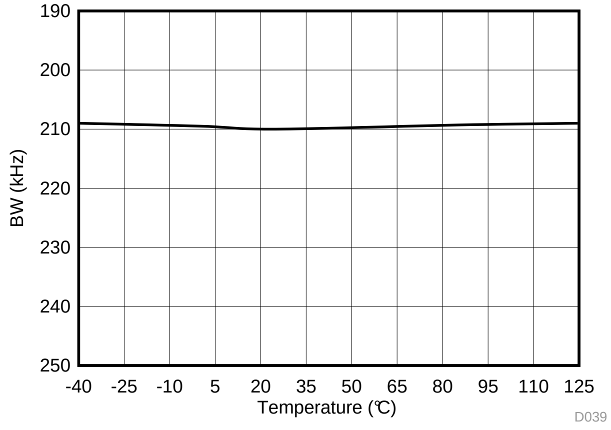


图 42. Output Bandwidth vs Temperature

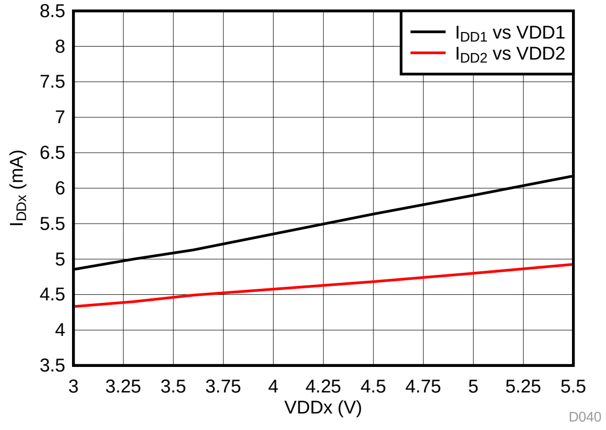


图 43. Supply Current vs Supply Voltage

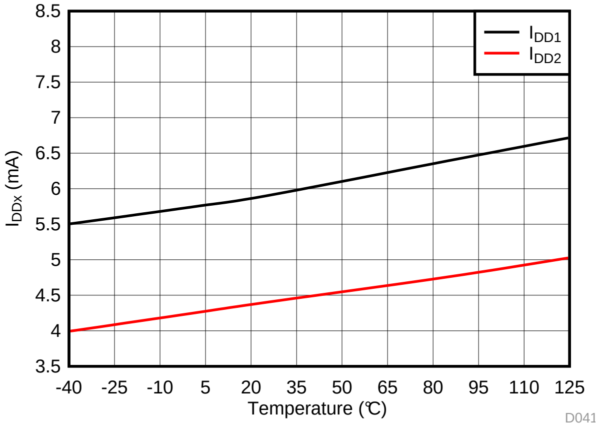


图 44. Supply Current vs Temperature

7 Parameter Measurement Information

7.1 Timing Diagrams

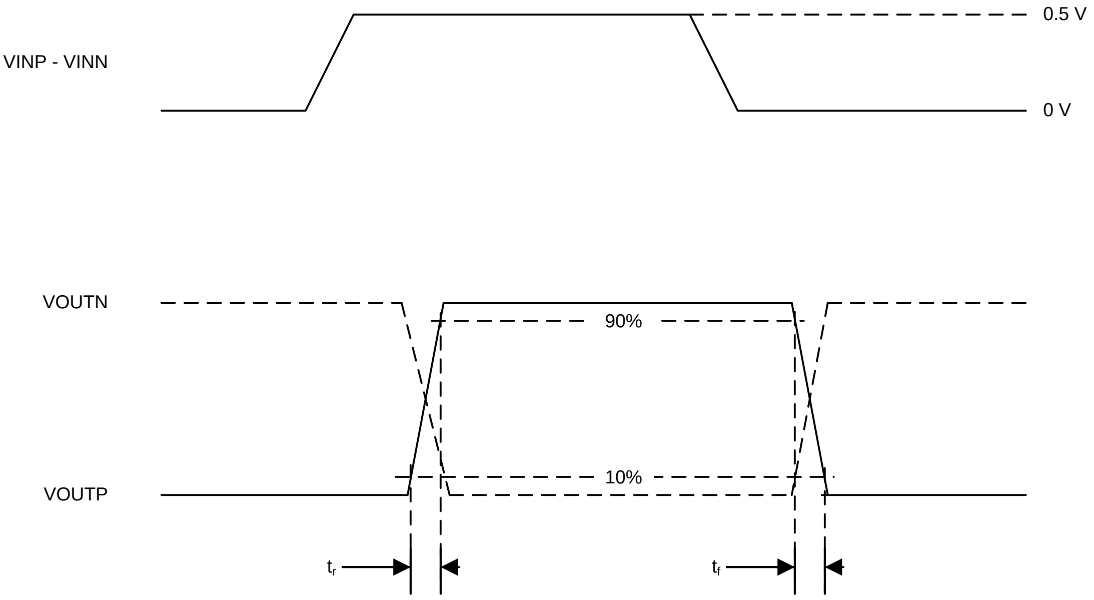


图 45. Rise and Fall Time Test Waveforms

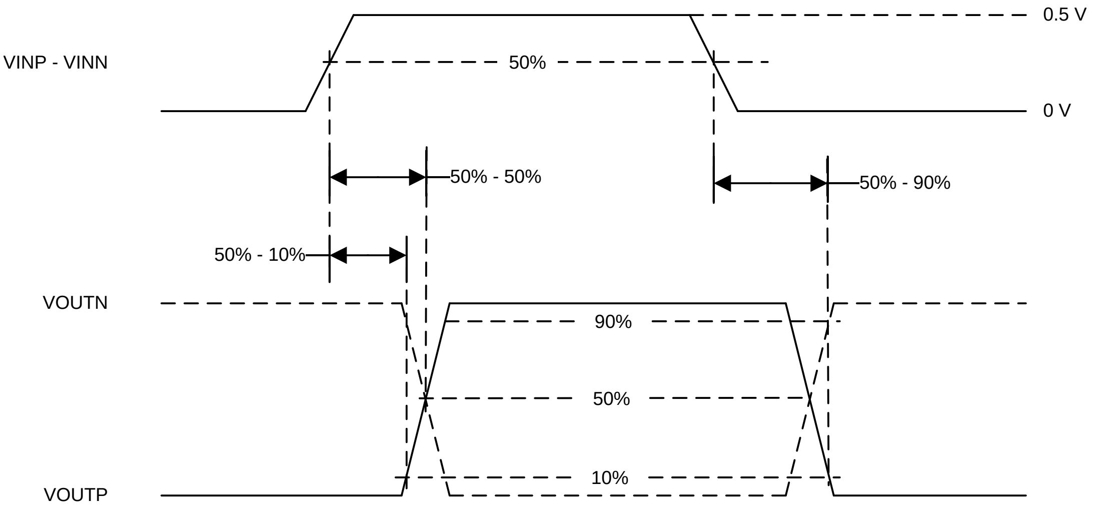


图 46. Delay Time Test Waveforms

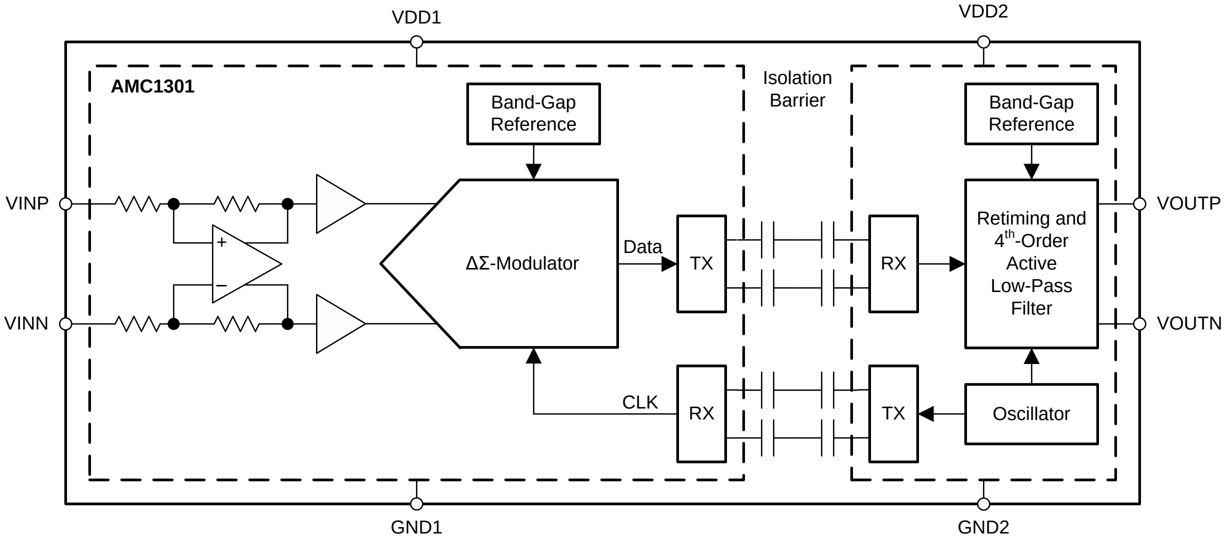
8 Detailed Description

8.1 Overview

The AMC1301 device is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully-differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (called *TX* in the *Functional Block Diagram*) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed by a fourth-order analog filter on the low-side and presented as a differential output of the device, as shown in the *Functional Block Diagram.*

The SiO_2-based, double-capacitive isolation barrier supports a high level of magnetic field immunity, as described in *ISO72x Digital Isolator Magnetic-Field Immunity*. The digital modulation used in the AMC1301 device and the isolation barrier characteristics result in high reliability and common-mode transient immunity.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Analog Input

The AMC1301 device incorporates front-end circuitry that contains a fully-differential amplifier followed by a ΔΣ modulator sampling stage. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 with a differential input impedance of 22 kΩ. Consider the input impedance of the AMC1301 device in designs with high-impedance signal sources that may cause degradation of gain and offset specifications. The importance of this effect, however, depends on the desired system performance.

Additionally, the input bias current caused by the internal common-mode voltage at the output of the differential amplifier causes an offset that is dependent on the actual amplitude of the input signal. See the *Isolated Voltage Sensing* section for more details on reducing this effect.

There are two restrictions on the analog input signals (VINP and VINN). First, if the input voltage exceeds the range GND1 – 6 V to VDD1 + 0.5 V, then the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) protection turns on. In addition, the linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

Feature Description (接下页)

8.3.2 Fail-Safe Output

The AMC1301 device offers a fail-safe output that simplifies diagnostics on system level. The fail-safe output is active in two cases:

- When the high-side supply VDD1 of the AMC1301 device is missing, or
- When the common-mode input voltage, that is V_{CM} = (VINP + VINN) / 2, exceeds the minimum common-mode over-voltage detection level V_{CMov} of VDD1 – 2 V.

The fail-safe output of the AMC1301 device is a negative differential output voltage value that differs from the negative clipping output voltage, as shown in 图 47 and 图 48. As a reference value for the fail-safe detection on a system level, use the $V_{FAILSAFE}$ maximum value of –2.545 V.

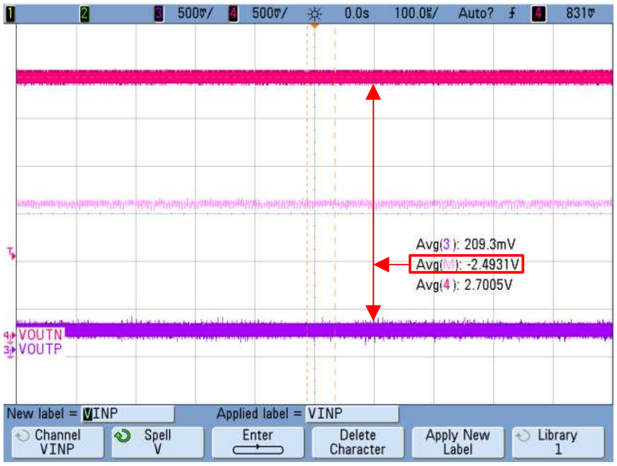

图 47. Typical Negative Clipping Output of the AMC1301 Device

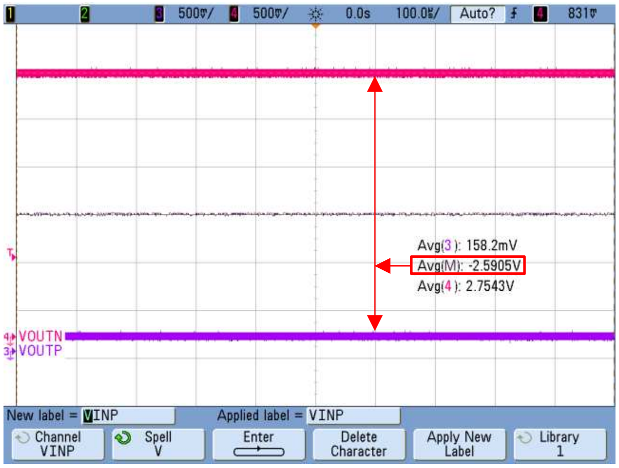

图 48. Typical Failsafe Output of the AMC1301 Device

8.4 Device Functional Modes

The AMC1301 device is operational when the power supplies VDD1 and VDD2 are applied, as specified in *Recommended Operating Conditions*.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The AMC1301 device offers unique linearity, high input common-mode and power-supply rejection, low ac and dc errors, and low temperature drift. These features make the AMC1301 device a robust, high-performance, isolated amplifier for industrial applications where high voltage isolation is required.

9.2 Typical Applications

9.2.1 Frequency Inverter Application

Isolated amplifiers are widely used in frequency inverters that are critical parts of industrial motor drives, photovoltaic inverters, uninterruptible power supplies, electrical and hybrid electrical vehicles, and other industrial applications. The input structure of the AMC1301 device is optimized for use with low-value shunt resistors and is therefore tailored for isolated current sensing using shunts.

图 49 shows a typical operation of the AMC1301 device for current sensing in a frequency inverter application. Phase current measurement is done through the shunt resistor, R_{SHUNT} (in this case, a two-pin shunt). The differential input and the high common-mode transient immunity of the AMC1301 device ensure reliable and accurate operation even in high-noise environments (such as the power stage of the motor drive).

Additionally, the AMC1301 device may also be used for isolated voltage measurement of the dc-link, as described in *Isolated Voltage Sensing*.

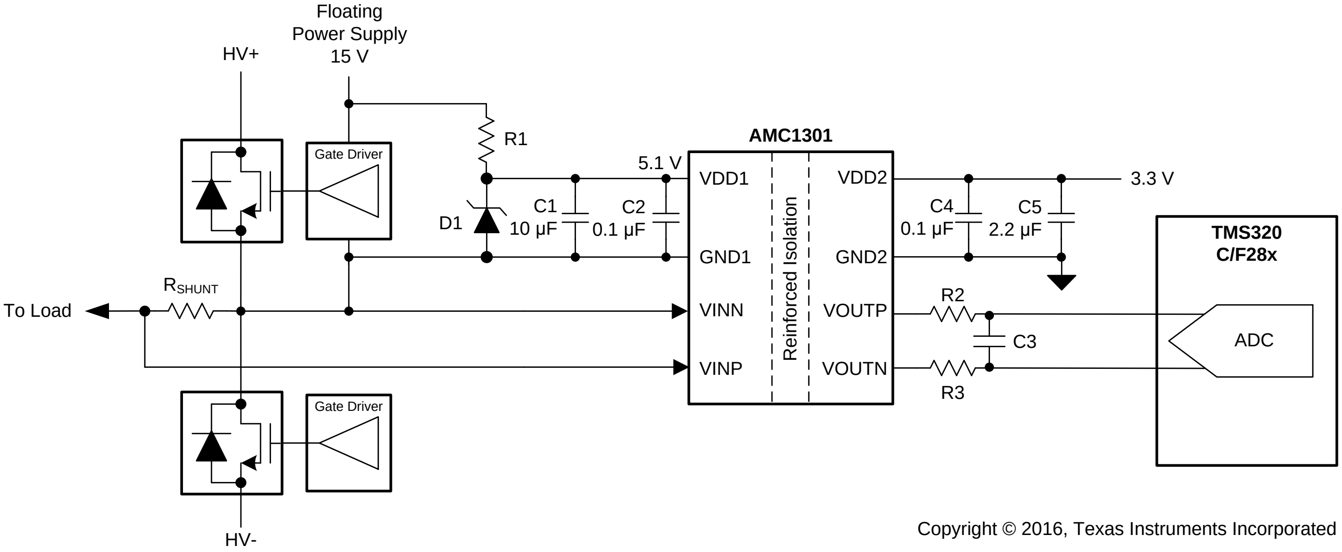

图 49. Using the AMC1301 Device for Current Sensing in Frequency Inverters

Typical Applications (接下页)

9.2.1.1 Design Requirements

表 1 lists the parameters for the typical application in 图 49.

表 1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across the shunt for a linear response	± 250 mV (maximum)

9.2.1.2 Detailed Design Procedure

The high-side power supply (VDD1) for the AMC1301 device is derived from the power supply of the upper gate driver. Further details are provided in the *Power Supply Recommendations* section.

The floating ground reference (GND1) is derived from one of the ends of the shunt resistor that is connected to the negative input of the AMC1301 device (VINN). If a four-pin shunt is used, the inputs of the AMC1301 device are connected to the inner leads and GND1 is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT}:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $V_{SHUNT} \leq \pm 250$ mV
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$

For best performance, use an RC filter (components R_2, R_3, and C_3 in 图 49) to minimize the noise of the differential output signal. Tailor the bandwidth of this RC filter to the bandwidth requirement of the system. TI recommends an NP0-type capacitor to be used for C_3.

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, consult the TI Precision Designs *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* (SLAU515) and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* (SLAU513), available for download at www.ti.com.

9.2.1.3 *Application Curves*

In frequency inverter applications, the power switches must be protected in case of an overcurrent condition. To allow for fast powering off of the system, a low delay caused by the isolated amplifier is required. 图 50 shows the typical full-scale step response of the AMC1301 device. Consider the delay of the required window comparator and the MCU to calculate the overall response time of the system.

图 50. Step Response of the AMC1301 Device

The high linearity and low temperature drift of offset and gain errors of the AMC1301 device, as shown in 图 51, allows design of motor drives with low torque ripple.

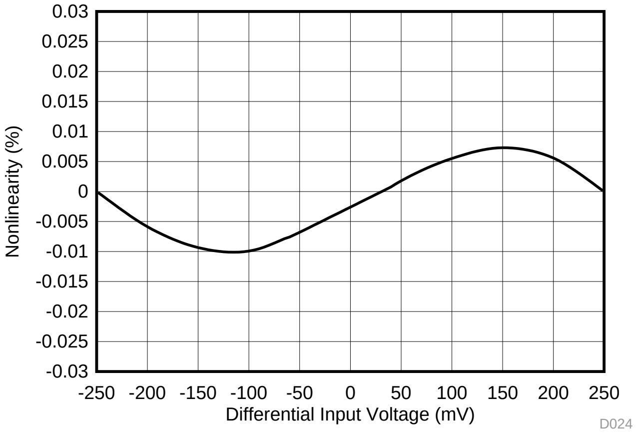

图 51. Typical Nonlinearity of the AMC1301 Device

9.2.2 Isolated Voltage Sensing

The AMC1301 device is optimized for usage in current-sensing applications using low-impedance shunts. However, the device may also be used in isolated voltage-sensing applications if the effect of the (usually higher) impedance of the resistor divider used in this case is considered.

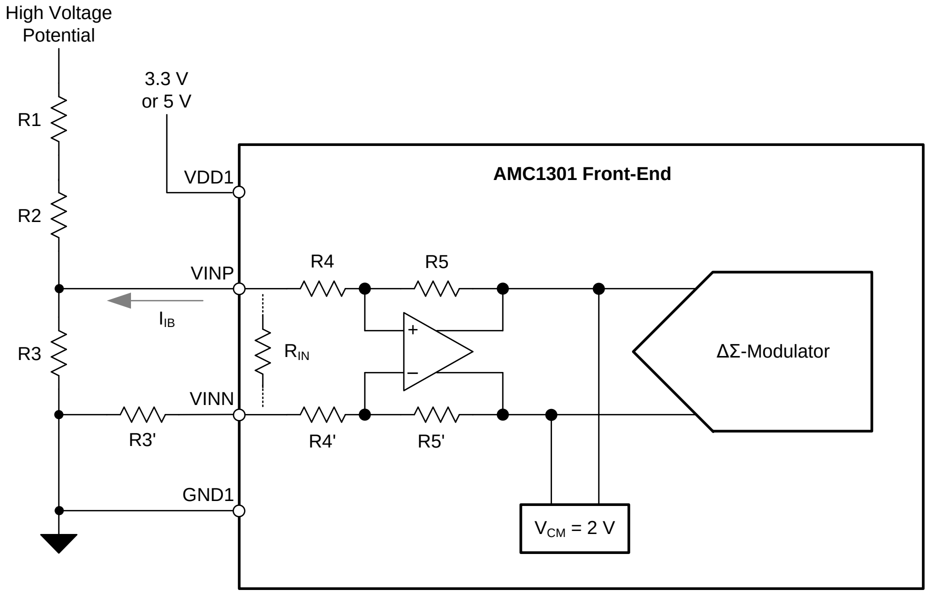

图 52. Using the AMC1301 Device for Isolated Voltage Sensing

9.2.2.1 Design Requirements

图 52 shows a simplified circuit typically used in high-voltage sensing applications. The high-impedance resistors (R1 and R2) dominate the current value that flows through the resistive divider. The resistance of the sensing resistor R3 is chosen to meet the input voltage range of the AMC1301 device. This resistor and the input impedance of the device (R_{IN} = 18 kΩ) also create a voltage divider that results in an additional gain error. With the assumption of R1 and R2 having a considerably higher value than R3 and omitting R3' for the moment, the resulting total gain error is estimated using 公式 1, with E_G being the initial gain error of the AMC1301 device.

$$\left|E_{Gtot}\right| = \left|E_G\right| + \frac{R_3}{R_{IN}} \quad (1)$$

This gain error may be easily minimized during the initial system-level gain calibration procedure.

9.2.2.2 Detailed Design Procedure

As indicated in 图 52, the output of the integrated differential amplifier is internally biased to a common-mode voltage of 2 V. This voltage results in a bias current I_{IB} through the resistive network R4 and R5 (or R4' and R5') used for setting the gain of the amplifier. The value of this current is specified in the *Pin Configuration and Functions* section. This bias current generates additional offset and gain errors that depend on the value of the resistor R3. Because the value of this bias current depends on the actual common-mode amplitude of the input signal (as shown in 图 53), the initial system offset calibration eliminates the offset but not the gain error component. Therefore, in systems with high accuracy requirements, a series resistor is recommended to be used at the negative input (VINN) of the AMC1301 device with a value equal to the shunt resistor R3 (that is, R3' = R3 in 图 52) to eliminate the effect of the bias current.

This additional series resistor (R3') influences the gain error of the circuit. The effect is calculated using 公式 2 with R4 = R4' = 12.5 kΩ. The effect of the internal resistors R5 = R5' cancels in this calculation.

$$E_G(\%) = \left(1 - \frac{R4}{R4' + R3'}\right) * 100\% \quad (2)$$

9.2.2.3 Application Curve

图 53 shows the dependency of the input bias current on the common-mode voltage at the input of the AMC1301 device.

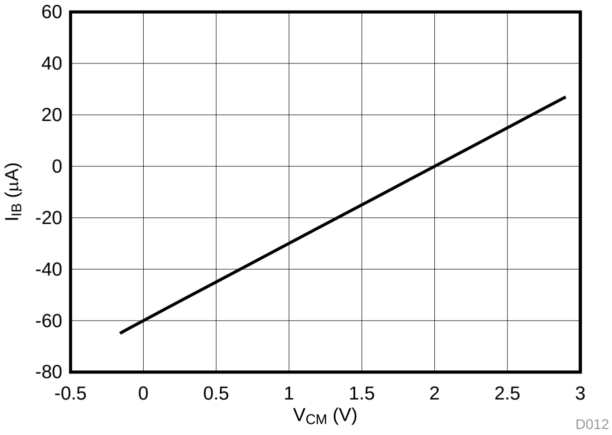

图 53. Input Current vs Input Common-Mode Voltage

9.3 Do's and Don'ts

Do not leave the inputs of the AMC1301 device unconnected (floating) when the device is powered up. If both device inputs are left floating, the input bias current drives them to the output common-mode of the analog front-end of approximately 2 V. If the high-side supply voltage VDD1 is below 4 V, the internal common-mode overvoltage detector turns on and the output functions as described in the *Fail-Safe Output* section, which may lead to an undesired reaction on the system level.

10 Power Supply Recommendations

In a typical frequency inverter application, the high-side power supply (VDD1) for the device is derived from the floating power supply of the upper gate driver. For lowest cost, a Zener diode may be used to limit the voltage to 5 V (or 3.3 V, depending on the design) ± 10%. Alternatively a low-cost, low-dropout (LDO) regulator (for example, the LM317-N) may be used to minimize noise on the power supply. TI recommends a low-ESR decoupling capacitor of 0.1 µF to filter this power-supply path. Place this capacitor (C_2 in 图 54) as close as possible to the VDD1 pin of the AMC1301 device for best performance. If better filtering is required, an additional 10-µF capacitor may be used. The floating ground reference (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (VINN) of the device. If a four-pin shunt is used, the device inputs are connected to the inner leads, and GND1 is connected to one of the outer leads of the shunt.

To decouple the digital power supply on the controller side, use a 0.1-µF capacitor placed as close to the VDD2 pin of the AMC1301 device as possible, followed by an additional capacitor from 1 µF to 10 µF.

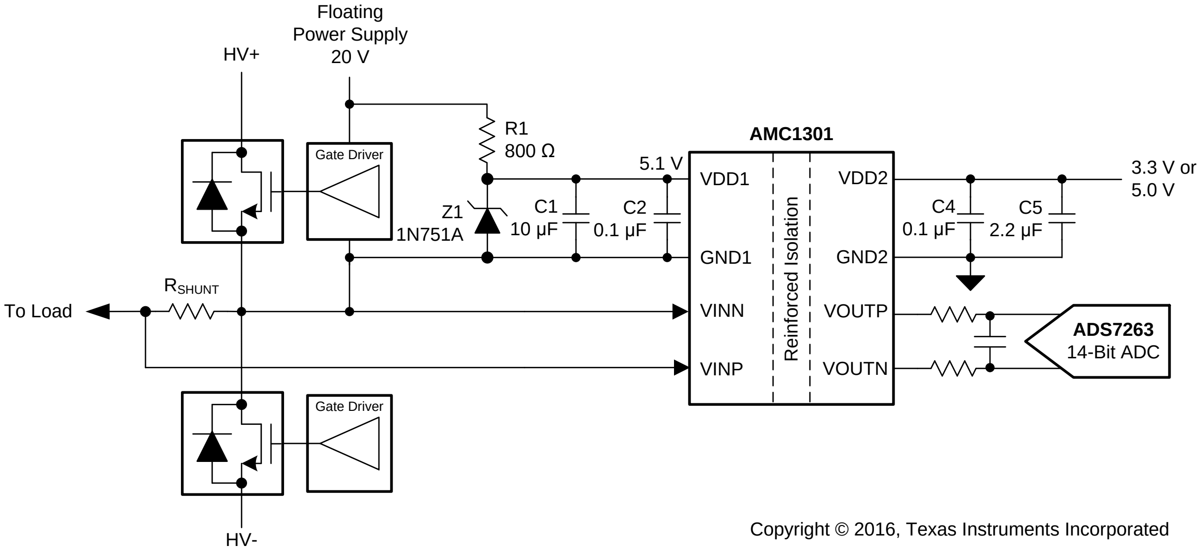

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图 54. Zener-Diode-Based, High-Side Power Supply

11 Layout

11.1 Layout Guidelines

A layout recommendation showing the critical placement of the decoupling capacitors (as close as possible to the AMC1301 device) and placement of the other components required by the device is shown in 图 55. For best performance, place the shunt resistor close to the VINP and VINN inputs of the AMC1301 device and keep the layout of both connections symmetrical.

11.2 Layout Example

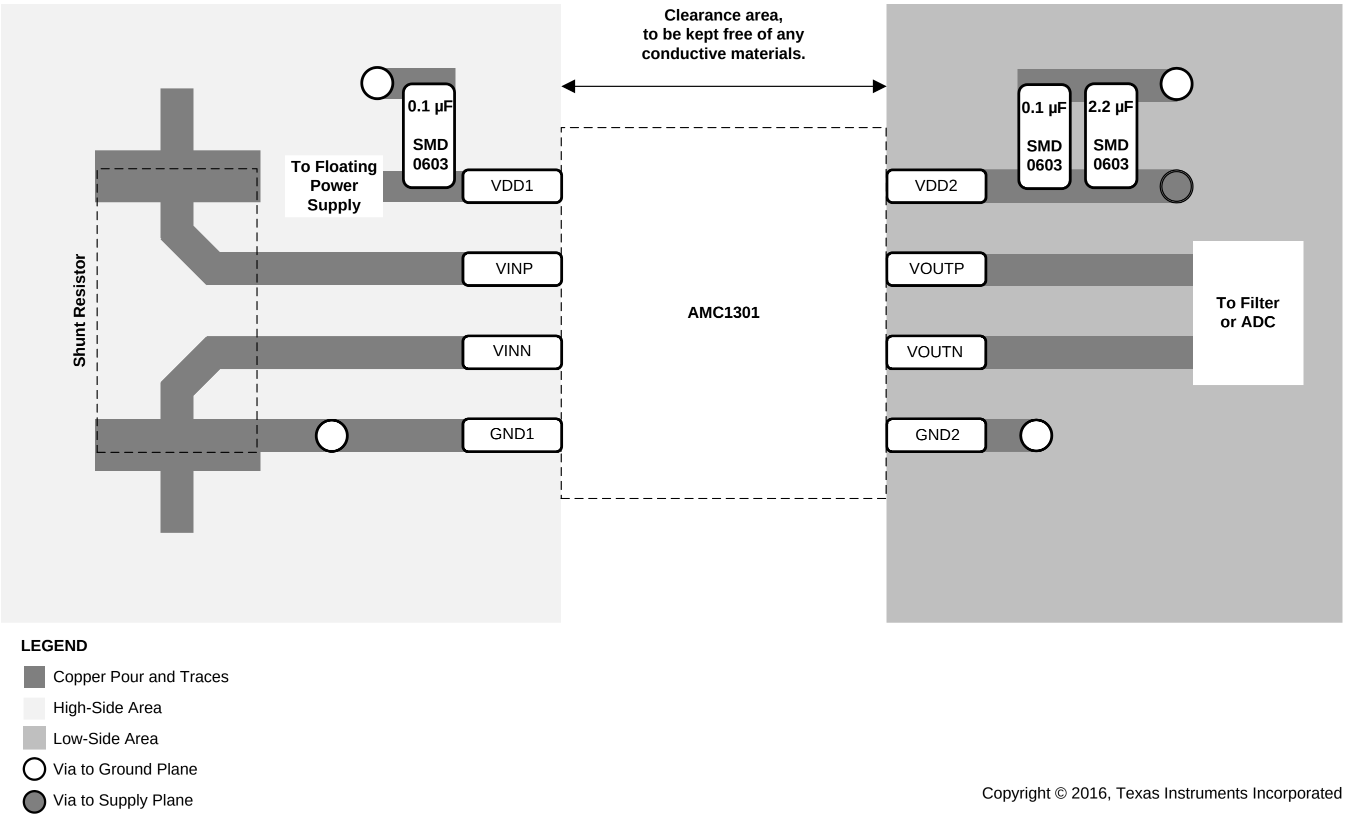

图 55. Recommended Layout of the AMC1301 Device

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- *隔离相关术语*
- *《双通道、1MSPS、16/14/12 位、4×2 或 2×2 通道同步采样模数转换器》*
- *《LM117、LM317-N 宽温度范围三引脚可调稳压器》*
- *《ISO72x 数字隔离器磁场抗扰度》*
- *《针对最低失真和最低噪声进行优化的 18 位 1MSPS 数据采集模块 (DAQ)》*
- *《针对最低功耗进行优化的 18 位 1MSPS 数据采集模块 (DAQ)》*

12.2 接收文档更新通知

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12.3 社区资源

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1301DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1301	Samples
AMC1301DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1301	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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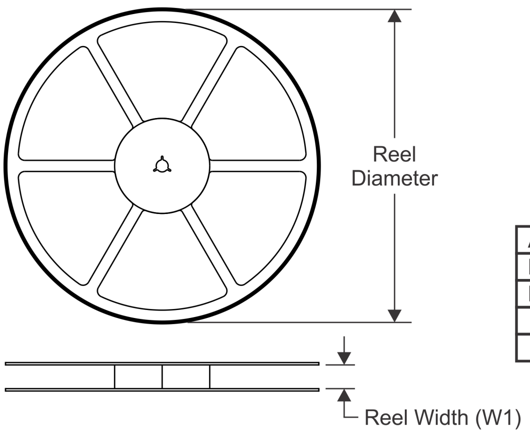
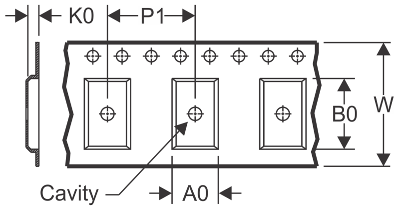
TAPE AND REEL INFORMATION

REEL DIMENSIONS

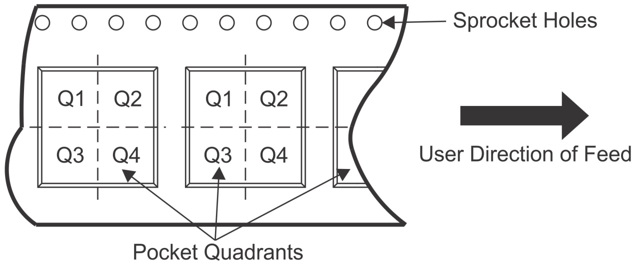


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

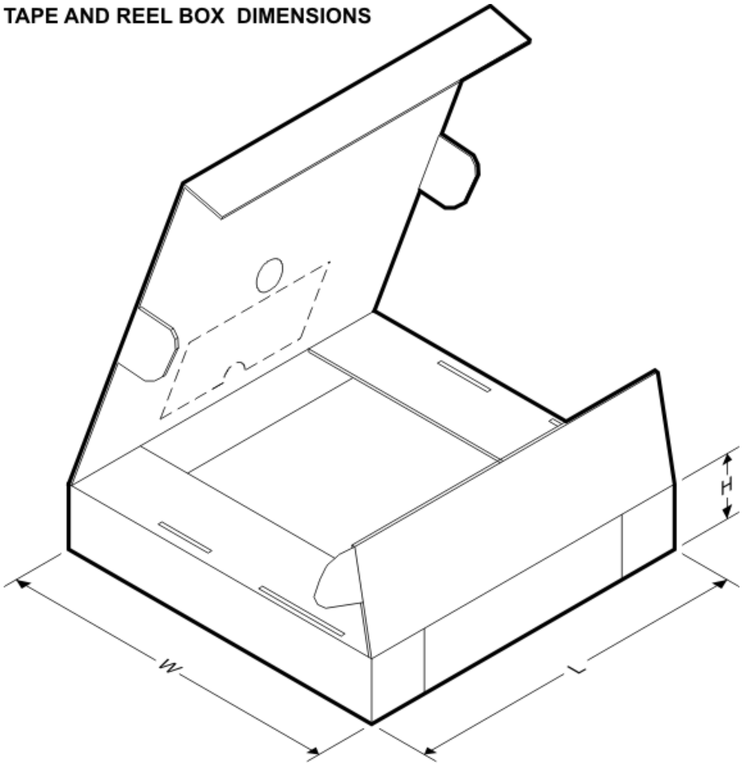
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1301DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

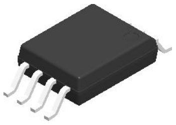
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

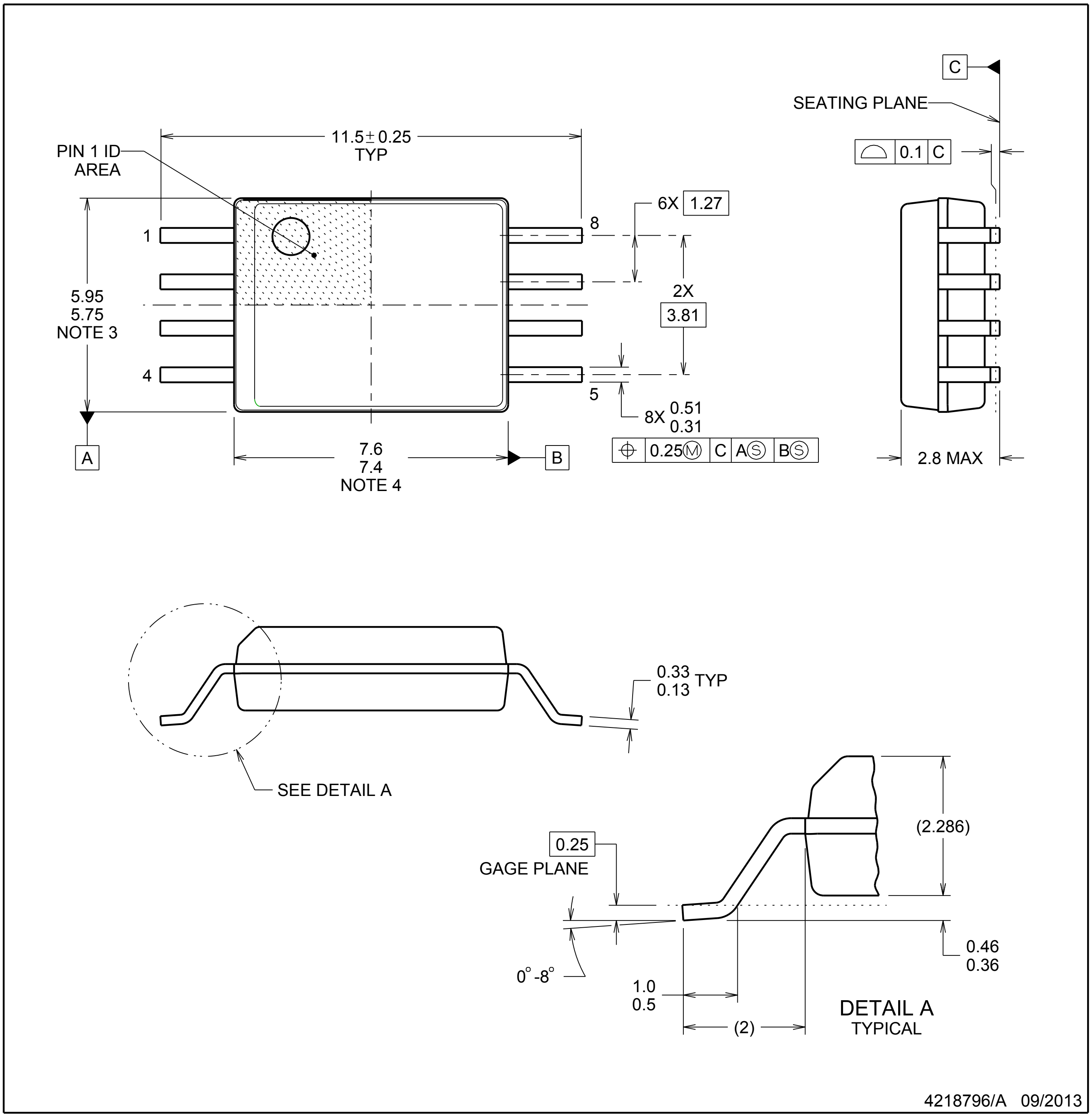
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1301DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0

DWV0008A



SOIC - 2.8 mm max height

SOIC



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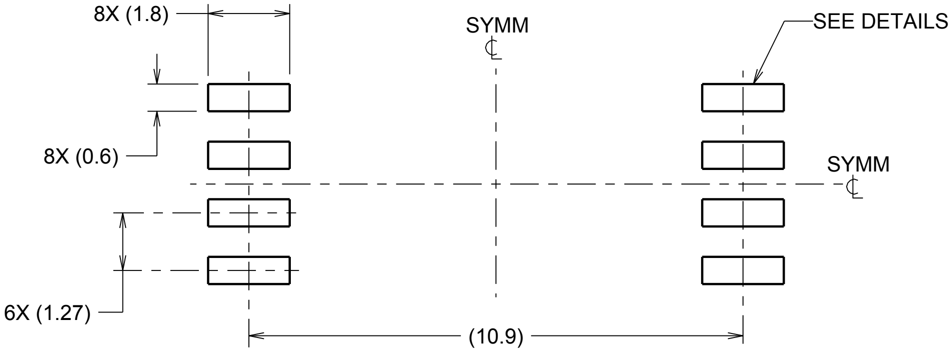
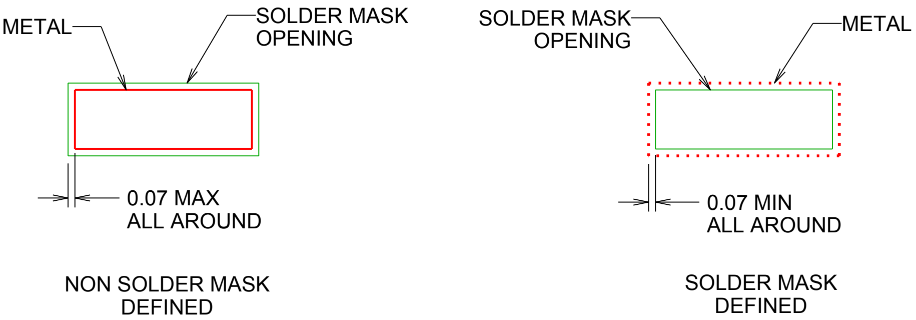
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

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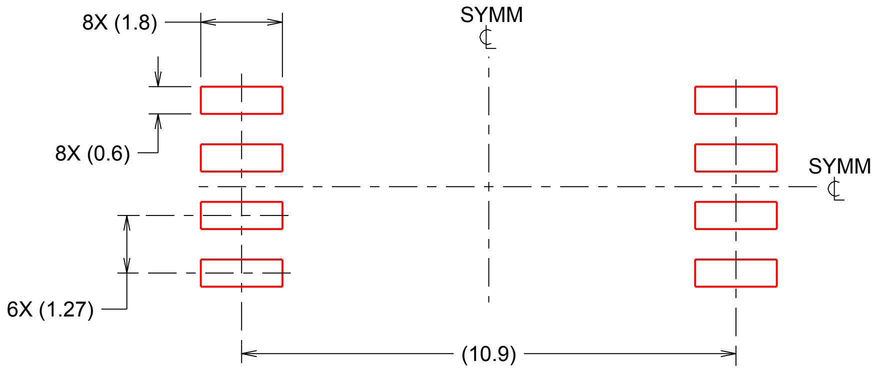
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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